IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A communication profiler, for use with a data processing system including a processor and a memory coupled by a system interconnect, wherein said communication profiler comprises:

a control unit including an input port coupled to said system interconnect, wherein said control unit receives a collection of data via said input port as a result of a tenure on said system interconnect, wherein said control unit filters said collection of data from said tenure to obtain specific data requested by a user and organizes said specific data as a summary, wherein said control unit filters said collection of data without perturbing the operation of said data processing system.

2. (original) The communication profiler according to claim 1, further comprising:

a profiler interconnect; and

a profiler memory, coupled to said profiler interconnect, wherein said profiler memory stored said summary.

3. (original) The communication profiler according to claim 1, further including:

an output port that can be coupled to an external analyzer to communicate said summary.

4. (original) The communication profiler according to claim 1, further comprising:

a control register, coupled to said control unit, which activates filtering of said collection of data by said control unit.

5. (original) The communication profiler according to claim 1, further including:

a transaction timer, coupled to said control unit, wherein said transaction timer is utilized to record a duration of a operation pending.

6. (original) The communication profiler according to claim 1, further comprising:

a data serializing and transmitting device that serially outputs said summary from said communication profiler, wherein said summary is indicative of normal hardware performance.

7. (currently amended) A data processing system, comprising:

a system interconnect;

a plurality of master elements, coupled to said system interconnect;

a plurality of slave elements, coupled to said system interconnect; and

a communication profiler, coupled to said system interconnect, further including: a control unit including an input port coupled to said system interconnect, wherein said control unit receives a collection of data via said input port as a result of a tenure between a master element and a slave element on said system interconnect, wherein said control unit filters said collection of data from said tenure and retrieves a set of specific data requested by a user and organizes said set of specific data as a summary, wherein said control unit filters said collection of data without perturbing the operation of said data processing system.

8. The data processing system according to claim 7, wherein said data processing system is a small computer system interface (SCSI) controller.

9. The data processing system according to claim 7, wherein said data processing system is implemented on a single integrated circuit substrate.

10. A host data processing system comprising:

a host interconnect;

a host processor coupled to said host interconnect;

a host memory coupled to said host interconnect;

a data processing system including a processor and memory coupled by a system interconnect comprising:

a plurality of master elements, coupled to said system interconnect;

a plurality of slave elements, coupled to said system interconnect; and

a communication profiler, coupled to said system interconnect, further including:

a control unit including an input port coupled to said system interconnect, wherein said control unit receives a collection of data via said input port as a result of a tenure between a master element and a slave element on said system interconnect, wherein said control unit filters said collection of data from said tenure and retrieves a set of specific data requested by a user and organizes said set of specific data as a summary, wherein said control unit filters said collection of data without perturbing the operation of said data processing system.

11. The host data processing system according to claim 10, further comprising:

a memory controller, coupled to said host interconnect, utilized to control said host memory.

12. A method for gathering hardware performance data, comprising the steps of:

activating a communication profiler coupled to a system interconnect by setting a control register, coupled to a control unit in said communication profiler;

monitoring a system interconnect for a tenure between a master element and a slave element of a data processing system, wherein said monitoring further includes filtering said collection of data without perturbing the operation of said data processing system; and

capturing a set of data resulting from said tenure and organizing said set of data into a summary, in response to detecting a tenure on said system interconnect.

13. The method for gathering hardware performance data according to claim 12, further comprising the step of:

deactivating said communication profiler, by resetting said control register.

14. The method for gathering hardware performance data according to claim 12, further comprising the step of:

transmitting said summary to an external analyzer.